

**REMARKS**

Claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34 and 35 are pending in this application. By this Amendment, claims 1, 4, 10 and 11 are amended. No new matter is added by these amendments. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

Claims 1, 4, 10 and 11 are objected to for informalities. Claims 1, 4, 10 and 11 are amended to obviate the objection. Accordingly, reconsideration and withdrawal of the objection to the above claims is respectfully requested.

Additionally, the Office Action rejects claims 1, 4, 5 and 8-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,567,484 to Hirota et al. (hereinafter "Hirota") and U.S. Patent No. 4,672,639 to Tanabe et al. (hereinafter "Tanabe"), and in further view of U.S. Patent No. 4,975,702 to Bazes; claims 16, 17, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Hirota, Tanabe and Bazes, and further in view of U.S. Patent No. 5,517,155 to Yamauchi et al. (hereinafter "Yamauchi"); claims 22 and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hirota, Tanabe and Yamauchi, and further in view of U.S. Patent No. 5,796,360 to Wendelrup; claims 25, 26, 31 and 32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hirota, Tanabe and Bazes, and further in view of U.S. Patent No. 6,477,181 to Fujimori et al. (hereinafter "Fujimori"); and claims 28, 29, 34 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hirota, Tanabe, Bazes and Fujimori, and further in view of what is asserted to be Applicant's admitted prior art. The Applicant respectfully traverses these rejections.

In asserting the prior art rejections listed above, the Office Action concedes that Hirota does not teach that the selected clock has been used as a sampling clock. The Office Action relies on Tanabe for this deficiency of Hirota. Further, the Office Action concedes that Hirota and Tanabe, in some combination, fails to teach that there is a set-up time and a

holding time associated with first to N-th holding circuits. The Office Action attempts to rely on Bazes for this deficiency. This reliance is improper for the following reasons.

The Office Action, beginning at the bottom of page 5, asserts that "Bazes discloses that the setup time requirement of the flip-flop is met if the signal has [been] stable for at least the setup time before the next transition of the SDL tap." However, this statement is incorrect. Bazes teaches in col. 5, lines 28-32, that the setup time requirement of the L-type flip-flop is met if the signal at the L-port of the L-type flip-flop has been stable for at least the setup time before the next transition of the SDL tap." Therefore, Bazes teaches that the control sample signals 46, 48 and 50 ( $L_{ADV}$ ,  $L_{MID}$  and  $L_{RET}$  in Fig. 4B) input to the L-ports of the flip-flops 54 are required to be stable for the setup and hold times of the flip-flops 54 instead of the clock signals TAP0 to TAP15 input to the clock terminals of the flip-flops 54.

Bazes teaches that the "clock signals TAP0 to TAP15 must be changed when a period equal to or greater than the setup time  $t_s$  has elapsed after the control sample signals 46, 48 and 50 changed," and "the control sample signals 46, 48 and 50 must be changed when a period equal to or greater than the hold time  $t_h$  has elapsed after the clock signals TAP0 to TAP15 changed." Therefore, Bazes teaches the relationship between the control sample signals 46, 48 and 50 and the setup and hold times of the flip-flops 54, but is silent about the relationship between the number N of taps of the clock signals TAP0 to TAP15 and the setup and hold times of the flip-flops 54. As such, the assertion of the Office Action that "inherently  $T_r/N$  must be equal or greater than  $(t_s + t_h)$ " is incorrect.

Further evidence of the impropriety of the above assertion is that Bazes proposes increasing the number N of taps as much as possible in order to increase the resolution as compared with the prior art example (col. 6, lines 1-22 of Bazes). As illustrated in Fig. 1 of Bazes, the resolution is  $t_r$ , which can be increased to  $t_r/N$ , thereby, the resolution increases as the number, N, of taps increases.

Therefore, the teachings of Bazes are in direct contradiction to the subject matter of the pending claims, which recites reducing the number of clocks  $N$  as much as possible, as evidenced by  $N \leq [T/(TS + TH)]$ . Specifically, when a high transfer rate is employed such as in a high-speed serial transfer, a person skilled in the art generally attempts to increase the number of clocks  $N$ , as disclosed by Bazes.

Hirota and Tanabe employ a method in which the amount of sampling information is increased by increasing the number of clocks  $N$  and sampling data using  $N$  clocks, and the change point is calculated based on the sampling information. However, this method results in an increase in the number of clocks  $N$ , whereby the circuit scale is increased.

The subject matter of the pending claims recites the number of clocks  $N$  is set at  $N \leq [T/(TS + TH)]$ . Specifically, while a person skilled in the art would attempt to increase the number of clocks  $N$  in order to deal with a high-speed transfer, the subject matter of the pending claims sets the number of clocks  $N$  to be equal to or less than  $[T/(TS + TH)]$ . Therefore, the number of holding circuits and the like can be reduced by setting the number of clocks  $N$  at  $N \leq [T/(TS + TH)]$ , whereby the circuit scale can be reduced.

Additionally, as discussed on pages 30-34, lines 4 to 12, respectfully, and illustrated by Figs. 12 to 14, of the Applicant's disclosure, when the number of clocks  $N$  is set at  $N > [T/(TS + TH)]$ , a situation indicated by D1 and D3 (Fig. 13A) occurs, whereby a number of undefined points occur, as indicated by D2 and D4. This creates a problem in which data cannot be appropriately sampled. However, the subject matter of the pending claims sets the number of clocks  $N$  at  $N \leq [T/(TS + TH)]$ , whereby the problem created by D2 and D4 can be prevented.

The applied references of Hirota, Tanabe, Yamauchi, Wendelrup, Fujimori and what is asserted to be Applicant's admitted prior art, do not overcome the deficiencies of Bazes as discussed above.

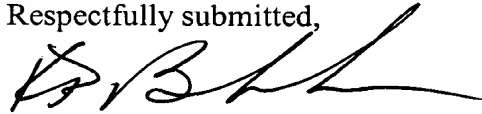
For at least the above reasons, the applied prior art references cannot reasonably be considered to teach, or to have suggested, the combinations of all of the features recited in at least independent claims 1 and 10. Further, claims 4, 5, 8, 9, 11-17, 19, 20, 22, 23, 25, 26, 28, 29,31, 32, 34 and 35 would also not have been suggested by the applied prior art references for at least the respective dependence of these claims on allowable independent claims 1 and 10, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29,31, 32, 34 and 35 under 35 U.S.C. §103(a) as being unpatentable over the combination of applied prior art references are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29,31, 32, 34 and 35 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Attachment:  
Request for Continued Examination

Date: August 14, 2007

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